Digital Modulator Megafunction

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Target Application:
Digital Signal Processing
Wireless Communications

Family:
FLEX 10K

Vendor:

NOVA ENGINEERING

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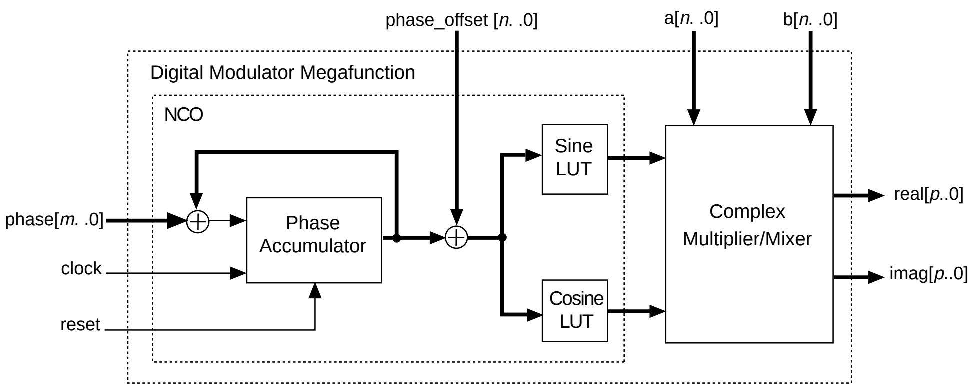
Features

- Optimized for the Altera® FLEX® 10K device architecture
- Parameterized complex multiplier/mixer
- Parameterized quadrature output numerically controlled oscillator (NCO)
- Configurable phase accumulator within the NCO
- Configurable phase offset input port
- Applications:
  - Amplitude modulation (AM)
  - Frequency modulation (FM)
  - Phase modulation
  - Down converters
  - Direct digital synthesis

General Description

The digital modulator megafunction from Nova Engineering contains a parameterized complex multiplier/mixer and quadrature output NCO. The NCO is a look-up table (LUT) that has a quadrature output, phase accumulator, and phase offset input port. The complex multiplier/mixer multiplies two user-defined inputs with the NCO outputs for amplitude modulation or frequency down conversion. Figure 1 shows a block diagram of the digital modulator megafunction.

Figure 1. Digital Modulator Megafunction Block Diagram



Functional Description

The NCO contains sine and cosine look-up tables (LUTs) that generate digital sine and cosine waveforms at a periodic rate. The LUTs perform the following functions:

$F_1[n] = \sin[2\pi n/N]$
$F_2[n] = \cos[2\pi n/N]$

where: n = Address input to the LUT
N = Number of samples in the LUT
$F_1[n]$ = Amplitude of sine wave at $[2\pi n/N]$
$F_2[n]$ = Amplitude of cosine wave at $[2\pi n/N]$

Incrementing n from 0 to N causes the LUT to output one complete cycle of amplitude values for the sine and cosine functions. The value $2\pi n/N$ represents a fractional phase angle between 0 ($n = 0$) and 2π ($n = N$). The time (t) required to increment n from 0 to N, is the period of the sine and cosine waveforms produced by the NCO. Moreover, an m-bit `phase` input generates the addresses for the quadrature NCO. The LUT address increments once each system clock cycle by an amount equal to the `phase` input. The LUT address, or phase angle, is accumulated and stored in the phase accumulator register. The register's output is used to address the sine and cosine LUTs.

The frequency (f) of the system clock (f_{CLOCK}) is fixed. Therefore, the frequency of the sine and cosine waves produced by the NCO is:

$$f = 1/T = (f_{CLOCK} \times \texttt{phase}) / 2^m$$

where: `phase` = Input phase angle

The `phase_offset` input modulates the NCO phase angle. The value from the `phase_offset` input is summed with the phase accumulator output. Both values, as well as the sum, are represented in two's complement format.

The complex multiplier/mixer can multiply two complex numbers represented in two's complement format. It uses a parallel-pipelined architecture that provides maximum speed. The complex multiplier/mixer performs the following function:

$$\texttt{real} + j\texttt{imag} = (\texttt{a} + j\texttt{b}) \times (\texttt{c} + j\texttt{d})$$

where:

$j = \sqrt{(-1)}$

$\texttt{real} = (a \times c) - (b \times d)$

$\texttt{imag} = (a \times d) + (b \times c)$

The total latency of the modulator from the `phase` input to the `real` output is 6 clock cycles. The output of the complex multiplier/mixer is registered to improve speed without increasing the number of logic cells used.

Ports

Table 1 describes the megafunction's ports.

Table 1. Digital Modulator Megafunction Ports

Name	Type	Size	Description
`phase` [m. . 0]	Input	12 to 32 bits	Specifies the NCO frequency in two's complement format.
`phase_offset`[n..0]	Input	1 to 10 bits	Specifies the NCO phase offset from 0° in two's complement format.
`a` [n . 0], `b` [n. . 0]	Input	1 to 8 bits	Complex data that are multiplied with the NCO outputs. Two's complement format.
`clock`	Input	–	System clock.
`reset`	Input	–	Asynchronous system reset, active high.
`real` [p. . 0]	Output	4 to 8 bits	Real part of complex result. Two's complement format.
`imag` [p. . 0]	Output	4 to 8 bits	Imaginary part of complex result. Two's complement format.

Parameters

Nova Engineering can customize the phase accumulator width, phase offset port width, NCO's LUT output width, and complex multiplier/mixer width to meet user specifications. The user can also request that functional blocks be removed or optionally bypassed. These custom-built parameters eliminate unnecessary logic and optimize the megafunction for specific applications.

Performance

Table 2 illustrates the device utilization and maximum clock frequency for a typical digital modulator megafunction in an EPF10K20-3 device. Custom configurations will differ in logic cell usage and performance.

Table 2. Typical Device Utilization for the Digital Modulator Megafunction in an EPF10K20-3 Device

Implementation	Clock (f_{MAX})	Logic Cells	EABs
`phase` = 24 bits; `phase_offset` = 10 bits; `a`, `b` = 8 bits; Outputs = 8 bits	35 MHz	662	2

Applications

The functional building blocks—the NCO, phase offset input port, and a complex multipler/mixer—allow the megafunction to implement a variety of modulators such as the amplitude, frequency, and phase modulators.

Amplitude Modulation

The designer begins by setting the NCO to a desired frequency. To program the NCO, the designer should select the appropriate `phase` word and system `clock` and set the `phase_offset` value to zero. The NCO will generate the desired sinusoidal waveform. The complex multiplier/mixer combines the NCO output with the `a` and `b` inputs. The output signal at the `real` port is:

$$\texttt{real}[p..0] = (a \times \cos(n)) - (b \times \sin(n))$$

Input `b` should be set to zero. The resulting AM sinusoid appears in two's complement form at the `real` output. The user can apply binary data to the most significant bit (MSB) of port `a` to create amplitude shift keying (ASK).

Quadrature amplitude modulation (QAM) is accomplished in a similar manner, except ports `a` and `b` are used to input the complex vector to be transmitted. The QAM signal appears at the `real` output in two's complement format.

Frequency Modulation

FM requires the user to modulate the `phase` input to the NCO. To program the NCO to the desired center frequency, select the appropriate `phase` word and system `clock` and set the `phase_offset` value to zero.

The data source can modulate the NCO frequency in several ways. After the data signals are digitized, they are added to the `phase` input. Each time the data changes, the `phase` input changes, which consequently changes the NCO frequency. The FM deviation, or maximum frequency change, can be controlled by scaling the data input. The maximum data value should correspond to a numerical value that increases the NCO frequency to the desired upper frequency limit. The minimum data value should correspond to the two's complement of the upper frequency limit. FM deviation and symmetry are accomplished by scaling the digital data source.

In addition, binary data can change the NCO frequency by controlling the multiplexers. Binary frequency shift keying (FSK) requires two `phase` words and a 2-to-1 multiplexer. A binary 1 selects one `phase` word and a binary 0 selects the other `phase` word to apply to the NCO. The serial binary data stream toggles the multiplexer to select one of the two `phase` words. Each selected `phase` word controls a desired NCO frequency. The user can also create an *M*-ary FSK by combining several bits to select one of *M* `phase` words. For example, a 8-ary FSK transmitter specifies one of 8 different frequencies to transmit on an 8-to-1 multiplexer using 3 select bits. The receiver then uses this frequency in a priority encoder to determine the 3 select bits.

Phase Modulation

Phase modulation is accomplished by imparting the data information onto the phase accumulator output. The `phase_offset` input port is provided for this purpose. To program the NCO to the desired frequency, select the appropriate `phase` word and system `clock`.

Binary phase shift keying (BPSK) is accomplished in the same way as FSK. That is, a 2-to-1 multiplexer selects one `phase_offset` word to apply to the `phase_offset` input port. In BPSK, the binary data transmitted can be applied to the MSB of the `phase_offset` input port. The user should set the `a` input to its maximum value and the `b` input to its minimum value (zero). The resulting BPSK waveform appears at the `real` output.

Quadrature phase shift keying (QPSK) is a composite of two BPSK waveforms in quadrature phase alignment. QPSK requires that the `a` and `b` inputs be set to the maximum value. It also requires a 4-to-1 multiplexer to select one `phase_offset` word to apply to the `phase_offset` input port. The resulting QPSK waveform appears at the `real` output port.

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